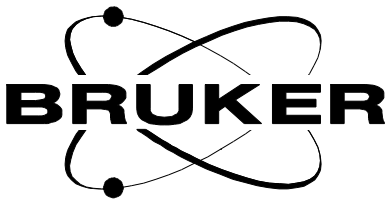


AQR ACB

Amplifier Control Board
User Manual

Version 003

BRUKER

The information in this manual may be altered without notice.

This manual was written by

G. Hiß

Rheinstetten, Germany

P/N: Z31224
DWG-Nr: 894003

Contents

Contents

Index

R

S

T

General 1

Overview 1.1

The ACB is designed to control up to eight amplifiers, using the SBS (Serial Bruker Spectrospin) protocol. It is the Interface between host computer (CCU) and the Bruker Linear Amplifiers (BLA).

Additionally the ACB prepares amplifier data for display on the BSMS keyboard. This display data contains, for each amplifier selected, forward and reflected power and a status byte. The display data can also be transferred via the RS232 interface to the host computer for display on the computer monitor.

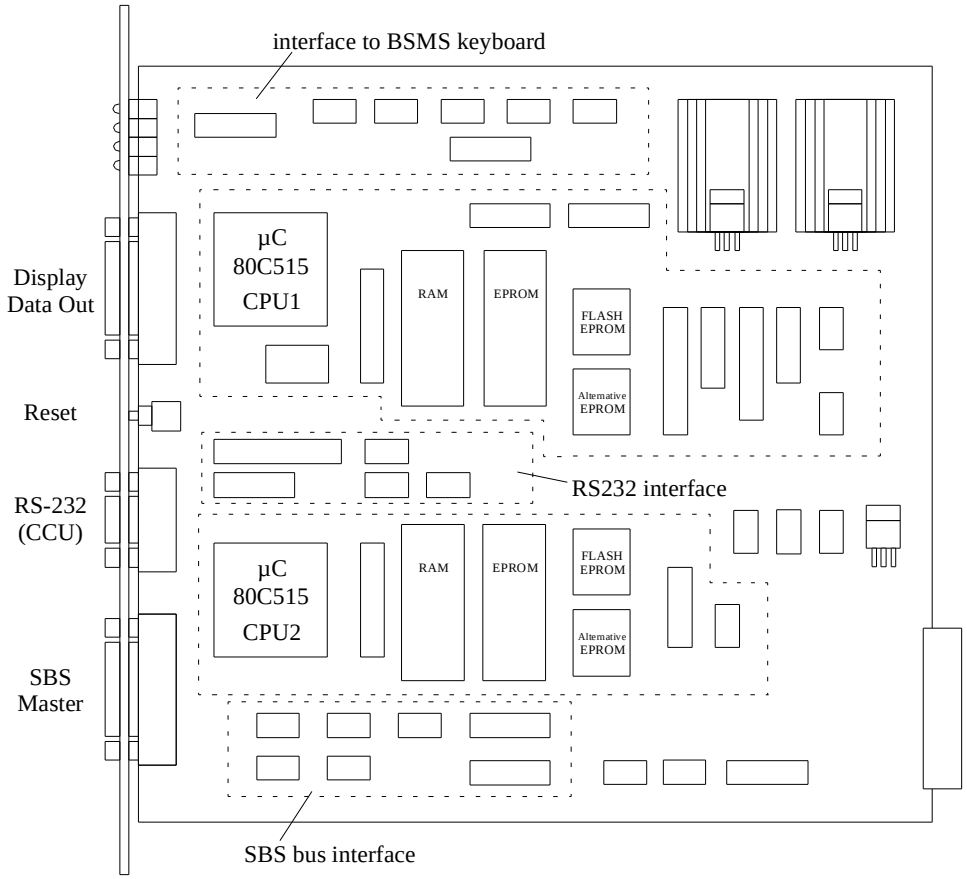
To perform a high refresh rate of the display data, the ACB is equipped with two separate micro controllers: one for data acquisition (CPU2) and the other (CPU1) for communication to the host computer.

Other features implemented on the ACB:

- Control of the Spectrometer Enable signal. The ACB turns off all selected linear amplifiers if the „Transmission Power Down“ button on the BSMS keyboard is pressed.
- On board BBIS (Bruker Board Information System).
- External I^2C bus, intended for communication with the BBIS of other AQR boards.

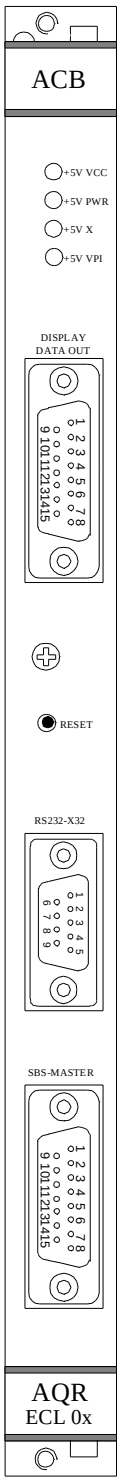
Layout *1.2*

Figure 1.1. ACB top view



Front panel *1.3*

Figure 1.2. ACB front panel



Voltage control (all of +5V). The LED lights if the corresponding voltage value exceeds 4.5 Volt.

Display Data Out
Provides the display data for the BSMS keyboard. It has a differential RS485 output.

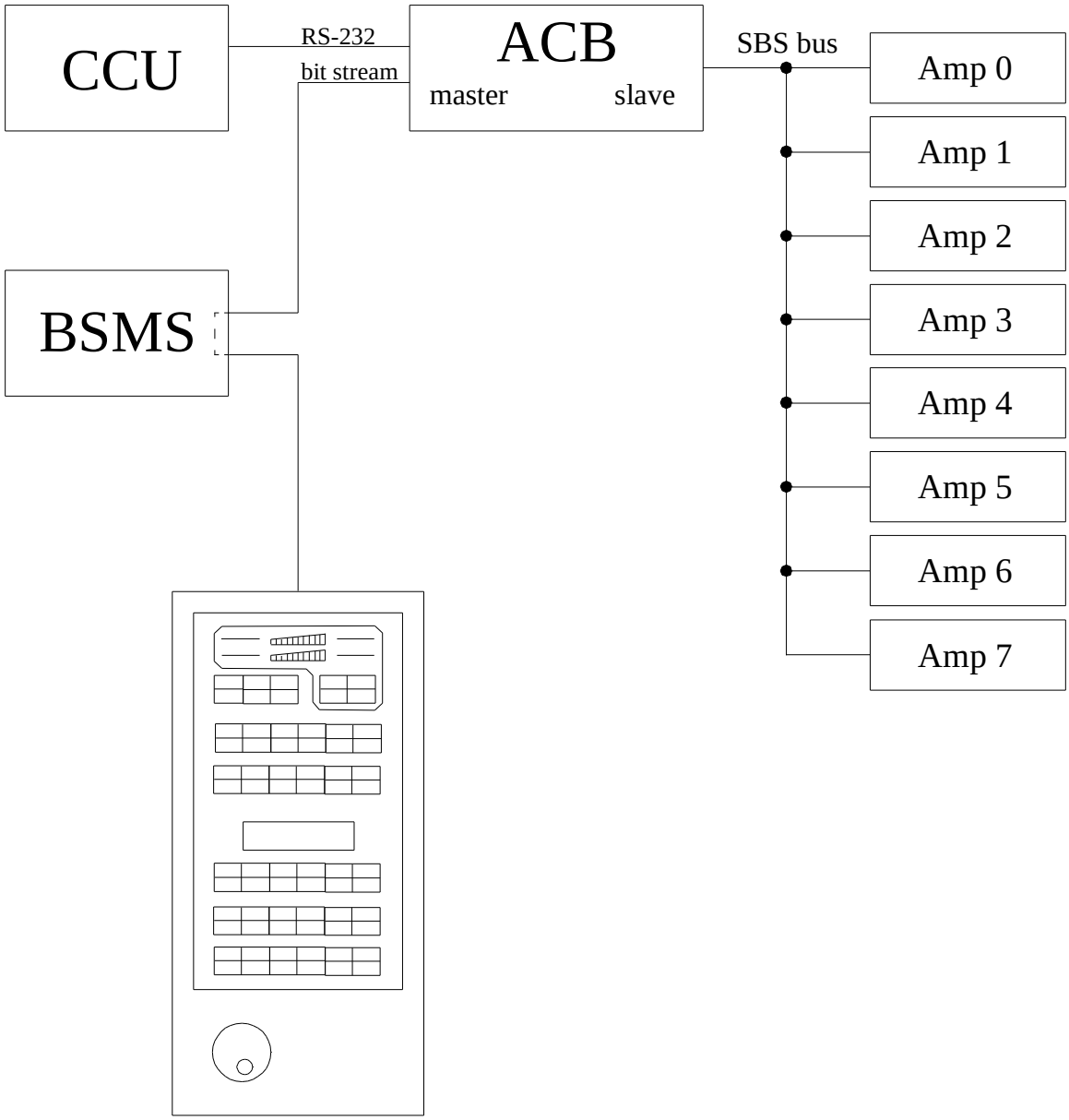
Reset switch

RS-232 interface to the host computer (CCU)

SBS bus Interface to the linear amplifiers with RS485 levels

Topology *1.4*

Figure 1.3. Topology ACB / Liner Amplifier (BLA)



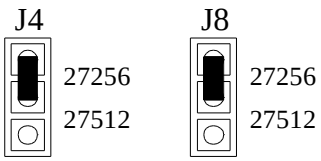
The ACB can interface up to 8 amplifiers via the SBS bus. Addressing is done using the hex switches placed on the front panel of each amplifier. The sequence in which the amplifier addresses are set is unimportant for the ACB. However all addresses must be different.

Installation 2

Jumpers 2.1

Before placing the ACB into the AQR Rack check the jumper settings. If an EPROM with 32 kByte (27256) is used J4 and J8 should be set as shown below:

Figure 2.1. jumper settings



The other jumpers (J1, J2, J3, J5, J6, J7) are not needed for this specific operation. If any of these jumper bases are present ensure that none is set.

Connections 2.2

The ACB must be situated in the AQR in the second slot from the right hand side.

- The ACB connector „RS232-X32“ is linked by the RS232 cable to a connector on the serial interface board (SIB) of the host computer.
- The ACB connector „SBS-MASTER“ is linked by the SBS bus cable to the amplifiers (BLA). The end of the bus cable must be terminated.
- The link to the BSMS keyboard is done via the 15 pin cable (delivered with the BSMS). This cable must connect the ACB connector, „Display Data Out“, with the BSMS CPU where the signals are brought through to the keyboard connector on the BSMS CPU. It contains both the lines for display data and the lines for the two switches next to the display.

IMPORTANT:

This cable must be attached before starting the spectrometer, otherwise several boards in the AQR (ASU, Router) will be disabled and the ACB reacts as if the TPD (Transmission Power Down) button were pressed turning off all amplifiers present.

Part numbers *2.3*

Table 2.1. Part Numbers

ACB	H5483
SBS Bus Cable	H5624
RS232 cable	HZ1482 (2m)
RS485 cable	delivered with BSMS
SBS terminator	H5167

Operation 3

Generating Display Data 3.1

After starting up the system the ACB scans all possible addresses on the SBS bus for amplifiers present. This operation takes a few seconds. Next the host computer requests the information about which amplifiers are present in the system, and starts an initialising sequence defining in the ACB which amplifiers are to be scanned and which amplifier's data should be displayed on the BSMS keyboard. Once this is done the ACB starts updating the BSMS keyboard display.

If a hard/software reset occurs the initialisation must be repeated.

Linear Amplifier Commands 3.2

If commands are to be given directly to the linear amplifiers the continuous scanning of the amplifiers must be interrupted. The ACB, therefore, contains a turn off command.

For application specific communication to the linear amplifiers the Multi Channel Commands must be used.

Using the service features (downloading of new firmware, etc.) the communication occurs in the usual way by using the Device Identifier of the corresponding linear amplifier.

TPD (Transmission Power Down) 3.3

A feature of the ACB is the control of the Spectrometer Enable Signal (!SPENAB). This line is present on the AQR back plane board and enables/disables particular AQR boards. Pressing the TPD button will cause the signal !SPENAB to go inactive (spectrometer disable) until the host computer reactivates it again with a command, or a hard/software reset occurs.

Hardware/Firmware 4

Hardware 4.1

The Hardware is divided to the following parts:

- CPU1 (communication)
- CPU2 (acquisition)
- external I^2C bus
- RS232 Interface to host computer (galvanically isolated)
- RS485 Interface to linear amplifiers (galvanically isolated)
- Interface to the BSMS keyboard (galvanically isolated)

CPU1 & CPU2 4.1.1

The organisational structure of both CPUs is identical so that the description here of CPU1 applies equally to CPU2.

The CPU is the micro controller 80C515AN from Siemens, clocked by a frequency of 18 MHz. For memory there are three chips in use:

1. EPROM(U15, DIL base)

   Either type 27C256 (32 kByte) or 27C512 (64 kByte) and contains the boot and download firmware.
   Alternatively to DIL the PLCC base (U17) can be used.

2. FLASH EPROM(U16, PLCC base)

   Type: 27F256 (32 kByte)
   Contains the application firmware

3. RAM(U14, DIL)

   Type: 62256 (32 kByte)

The use of Flash EPROMs enables new firmware to be downloaded without opening the unit, even by the customer.

Decoder (PAL) 4.1.2

The remainder of the PAL logic is used to decode the Memory section. The memory map is dependant on the signal PGMODE (Program Mode) at Pin P1.7 of the micro controller.

Table 4.1. Memory map

PGMODE	EPROM	FLASH	RAM
0 (applica-tion mode)	not mapped	Code 0x000-0x7FFF	Data 0x000-0x7FFF
1 (boot mode	Code 0x000-0x7FFF	Data 0x000-0x7FFF	not mapped

I²C E²Prom *4.1.3*

A serial E²Prom X24C16 (U22) with I²C bus-structure is used to store all BBIS (Bruker Board Information System) data. This chip is linked to both CPUs.

Interfaces *4.1.4*

All interfaces are galvanically isolated from the CPUs. These are:

RS-232 Interface

The basic serial interface hardware is integrated in the 80C515AN. The data and handshake lines are connected to port pins of the micro controller (U12) or to the separate output port (U20). After the galvanic isolation the lines are brought to RS232 levels.

Table 4.2. RS-232 interface

Signal name	Meaning	Sent by
!RxD	receive data	host computer
!TxD	transmit data	ACB
CTS	clear to send	host computer
RTS	request to send	ACB
DSR	data set ready	host computer
DTR	data terminal ready	ACB

RS-485 Interface

Used for communication with the linear amplifiers.

Table 4.3. RS-485 interface

Signal name	Meaning	Sent by
RxD+ RxD-	receive data pos. receive data neg.	amplifier
TxD+ TxD-	transmit data pos. transmit data neg.	ACB
!WUP	wake up line	ACB

Interface to the BSMS keyboard containing TPD

All signals have RS485 levels..

Table 4.4. interface to BSMS keyboard

Signal name	Meaning	Sent by
DATA+ DATA-	serial display data pos./neg.	ACB
CLOCK+ CLOCK-	clock signal pos./neg.	ACB
STROBE+ STROBE-	strobe signal pos./neg.	ACB
TOGGLE+ TOGGLE-	toggle of power indicator pos. /neg.	keyboard
TPD+ TPD-	Transmission Power Down pos. /neg.	keyboard

External I^2C bus

This bus is used for access to serial E^2PROMS placed on other boards in the AQR.

Table 4.5. external I^2C bus

Signal name	Meaning	Sent by
SDA	serial data	bidirectional
SCL	serial clock	ACB
SDIR	serial direction 0 : transmit 1 : receive	ACB

Firmware 4.2

Each CPU in the ACB contains two independent software modules; the boot firmware and the application firmware.

Boot firmware (CPU1 & CPU2) 4.2.1

The boot firmware controls the reset sequence and the downloading of new firmware releases. After initialisation, it checks if there is a valid application firmware stored on the Flash EPROM. If all tests are good, it switches to the application program by driving pin PGMODE to low. This causes the memory decoder to use the Flash EPROM as code memory and the RAM as data memory. The application program can now run.

While the boot program is running, the memory decoder maps the PROM as code memory and the Flash EPROM as Data memory (only data memory can be written by micro controller). As RAM, only the internal memory of the micro controller is used.

Application firmware 4.2.2

All application specific functions for the ACB are controlled by the application program. After the initialisation in both CPUs has been completed the programs run their main loops executing the following program parts:

CPU1 (communication CPU, master)

main functions:

- Command interpreter for all SBS commands.
- CPU link to CPU2 for display data.
- CPU link to CPU2 for SBS commands.
- Conversion and transmission of display data to the BSMS keyboard.
- Storage of display data available, on request, to the host computer.

CPU2 (acquisition CPU, slave)

main functions:

- Command interpreter for all SBS commands via the CPU link.
- Polling of the amplifiers selected for forward and reflected power and their status.

Connector Pinout 5

Display Data Out 5.1

15 pin Mini-D female

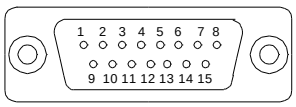


Table 5.1. Pinout - Display Data Out

Pin No.	Pin Name
1	PGND
2	-
3	DATA+
4	CLOCK+
5	STROBE+
6	TOGGLE+
7	TPD+
8	PGND
9	-
10	DATA-
11	CLOCK-
12	STROBE-
13	TOGGLE-
14	TPD-
15	+10V

RS-232 5.2

9 pin Mini-D male

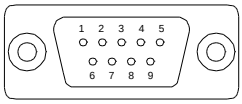


Table 5.2. Pinout - RS232

Pin No.	Pin Name
1	-
2	!RxD
3	!TxD
4	DTR
5	XGND
6	DSR
7	RTS
8	CTS
9	-

SBS Master 5.3

15 pin Mini-D female

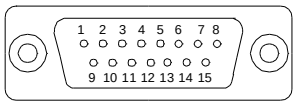


Table 5.3. Pinout - SBS Master

Pin No.	Pin Name
1	DI_GND9V
2	RxD+
3	!WUP
4	TxD+
5	-
6	DI_GND9V

Table 5.3. Pinout - SBS Master

Pin No.	Pin Name
7	DI_GND9V
8	DI_GND9V
9	RxD-
10	-
11	TxD-
12	-
13	DI_P9V
14	DI_P9V
15	DI_P9V

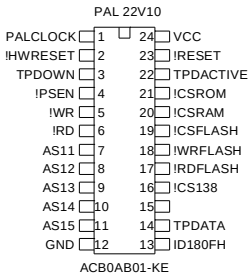
Connector Pinout

PAL listings

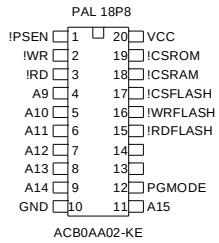
A

ACB0AB01-KE (PAL U18)

ACB0AA02-KE (PAL U38)




```
*IDENTIFICATION
 ACB0AB01-KE      14.07.1993      CS:7128
 Günther Hiß
 Bruker Elektronik GmbH

 design function :
 - Generation of CS-signals for RAM, EPROM, FLASH and 74S138.
 - Realisation of a D-FlipFlop with asynchronous set/reset input
   to storage the signal !SPENABLE (TPD).

*X-NAMES
 HWRESET,
 PSEN,WR,RD,A[15..11],           ! Address decoder
 PGMODE,                         ! Address decoder
 TPDDATA,                        ! Set/Reset FlipFlop with DATA
 TPDOWN,PALCLOCK;                ! Spectrometer Enable FlipFlop

*Y-NAMES
 CSROM,CSRAM,CSFLASH,            ! Address decoder
 WRFLASH,RDFLASH,CS138,          ! Address decoder
 TPDNEG,                         ! Set 1 if TPD button is pressed
 TPDACTIVE,                      ! TPDNEG inverted
 RESET;

*FUNCTION-TABLE
 $(A[15..11]), PGMODE, PSEN : CSROM, CSFLASH, CSRAM, CS138;
   0H..1FH   ,   1   ,  -   :   0  ,    0   ,   1  ,   1  ;
   0H..1EH   ,   0   ,  -   :   1  ,    0   ,   0  ,   1  ;
     1FH     ,   0   ,  0   :   1  ,    0   ,   1  ,   1  ;
     1FH     ,   0   ,  1   :   1  ,    1   ,   1  ,   0  ;
     REST                   :   1  ,    1   ,   1  ,   1  ;

 $(A[15..11]), PGMODE, RD , WR , PSEN : RDFLASH, WRFLASH;
   0H..1FH   ,   1   ,  1 ,  0 ,   1  :   1    ,    0   ; write flash D
   0H..1FH   ,   1   ,  0 ,  1 ,   1  :   0    ,    1   ; read flash  D
   0H..1FH   ,   0   ,  1 ,  1 ,   0  :   0    ,    1   ; read flash  C
     REST                             :   1    ,    1   ;

*BOOLEAN-EQUATIONS
 RESET = HWRESET;
 TPDNEG := /TPDDATA;
 TPDNEG.RS = TPDOWN;
 TPDACTIVE = /TPDNEG;

*SPECIAL-FUNCTIONS
 TPDNEG.INV = NO;
 TPDNEG.REG = YES;

*RUN-CONTROL
 LISTING = PLOT, EQUATIONS, PINOUT, SYMBOLTABLE, NETTABLE; LONG;
 PROGFORMAT = JEDEC;

*PLD
 TYPE = AMPAL22V10;

*PIN
 PALCLOCK=1, TPDOWN=3,                        ! Inputs
 TPDDATA=14, HWRESET=2,
 PSEN=4, WR=5, RD=6,
 A11=7, A12=8, A13=9, A14=10, A15=11,
 PGMODE=13,
 RESET=23,                                    ! Outputs
 CSROM=21, CSRAM=20, CSFLASH=19,
 WRFLASH=18, RDFLASH=17, CS138=16,
 TPDACTIVE=22,
 TPDNEG=15;

*END
```




```
*IDENTIFICATION
 ACB0AA02-KE      14.07.1993      CS:2AA8
 Günther Hiß
 Bruker Elektronik GmbH

 design function :
 - Generation of CS-signals for RAM, EPROM and FLASH.

*X-NAMES
 PSEN,WR,RD,A[15..9],
 PGMODE;

*Y-NAMES
 CSROM,CSRAM,CSFLASH,
 WRFLASH,RDFLASH;

*FUNCTION-TABLE
 $(A[15..9]), PGMODE, PSEN : CSROM, CSFLASH, CSRAM;
   0H..7FH  ,   1   ,  -   :   0  ,    0   ,   1  ;
   0H..7FH  ,   0   ,  -   :   1  ,    0   ,   0  ;
      REST               :   1  ,    1   ,   1  ;

 $(A[15..9]), PGMODE, RD , WR , PSEN : RDFLASH, WRFLASH;
   0H..7FH  ,   1   ,  1 ,  0 ,   1  :   1    ,    0   ; write flash D
   0H..7FH  ,   1   ,  0 ,  1 ,   1  :   0    ,    1   ; read flash  D
   0H..7FH  ,   0   ,  1 ,  1 ,   0  :   0    ,    1   ; read flash  C
      REST                           :   1    ,    1   ;

*RUN-CONTROL
 LISTING = PLOT, EQUATIONS, PINOUT, SYMBOLTABLE, NETTABLE; LONG;
 PROGFORMAT = JEDEC;

*PLD
 TYPE = AMPAL18P8;

*PIN
 PSEN=1,WR=2,RD=3,
 A9=4,A10=5,A11=6,A12=7,A13=8,A14=9,A15=11,
 PGMODE=12,
 RDFLASH=15,WRFLASH=16,
 CSFLASH=17,CSRAM=18,CSROM=19;

*END
```

Schematics

B

AQR Amplifier Control Board - Root

AQR Amplifier Control Board - RS232 Interfacep

AQR Amplifier Control Board - Bit Stream

AQR Amplifier Control Board - Power

AQR Amplifier Control Board - CPU1

AQR Amplifier Control Board - CPU2

AQR Amplifier Control Board - SBS-Bus

AQR Amplifier Control Board - Spare parts

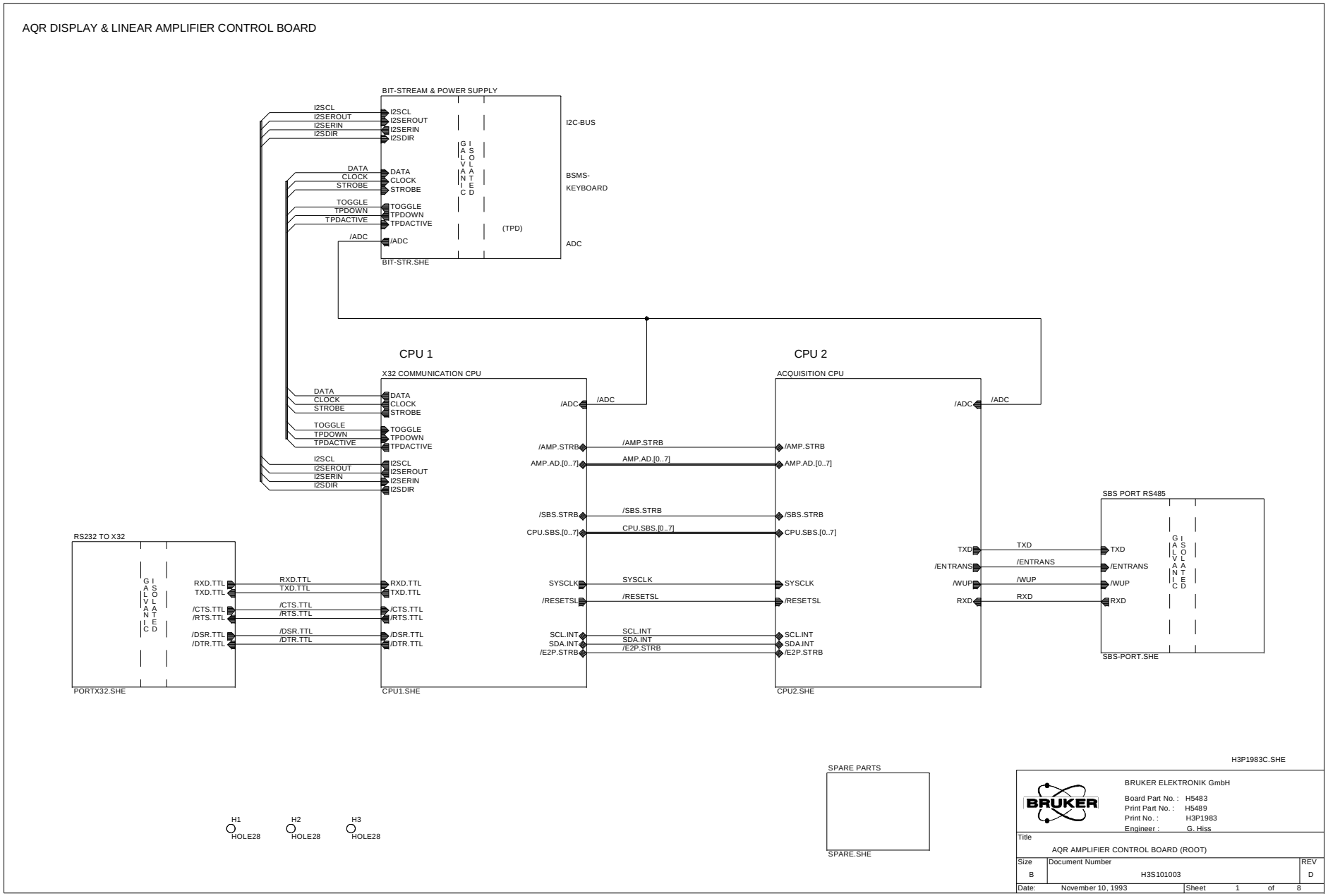


Figure B.1. ACB - Root

Figure B.2. ACB - RS232 Interface

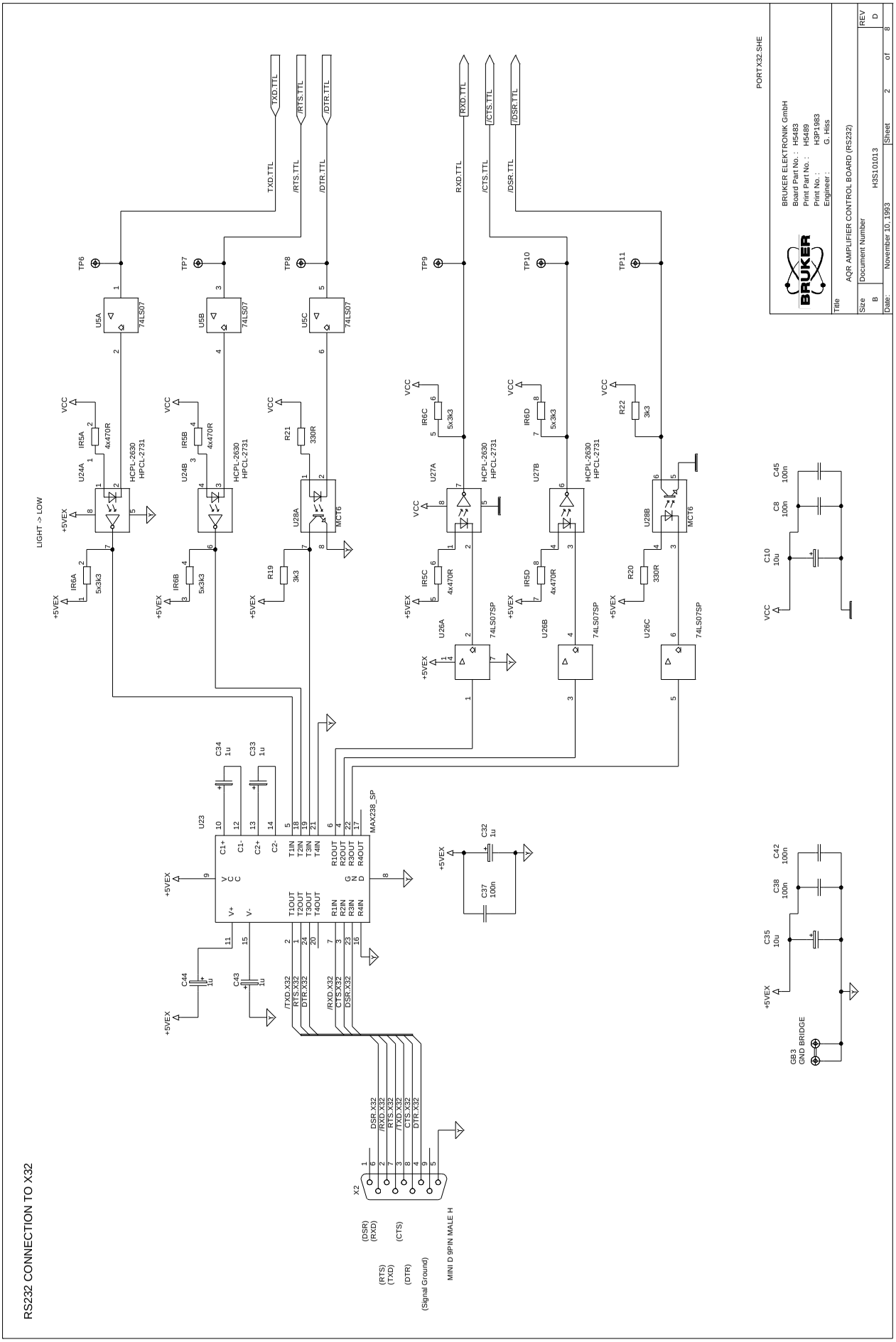
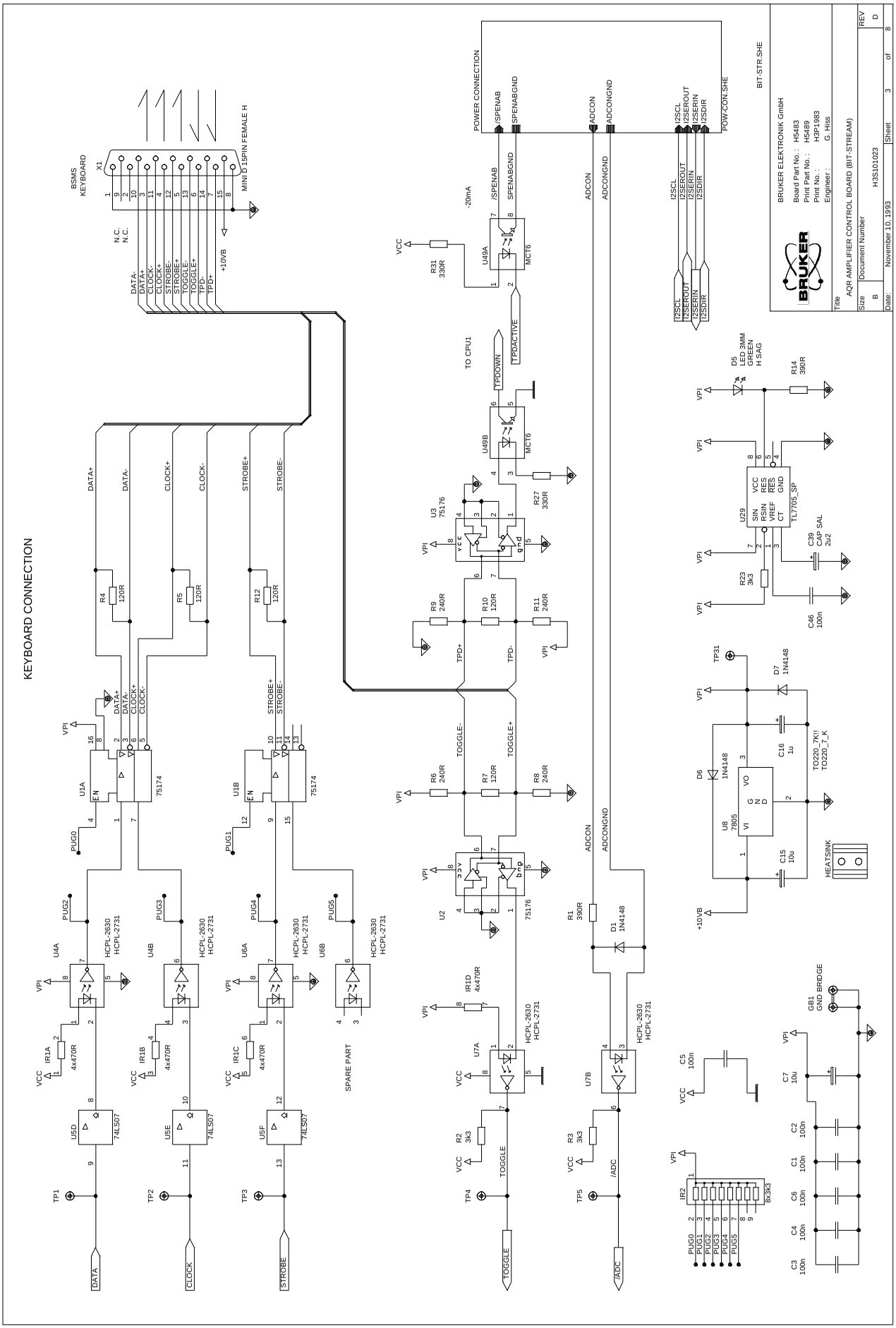


Figure B.3. ACB - bit stream to BSMS-keyboard



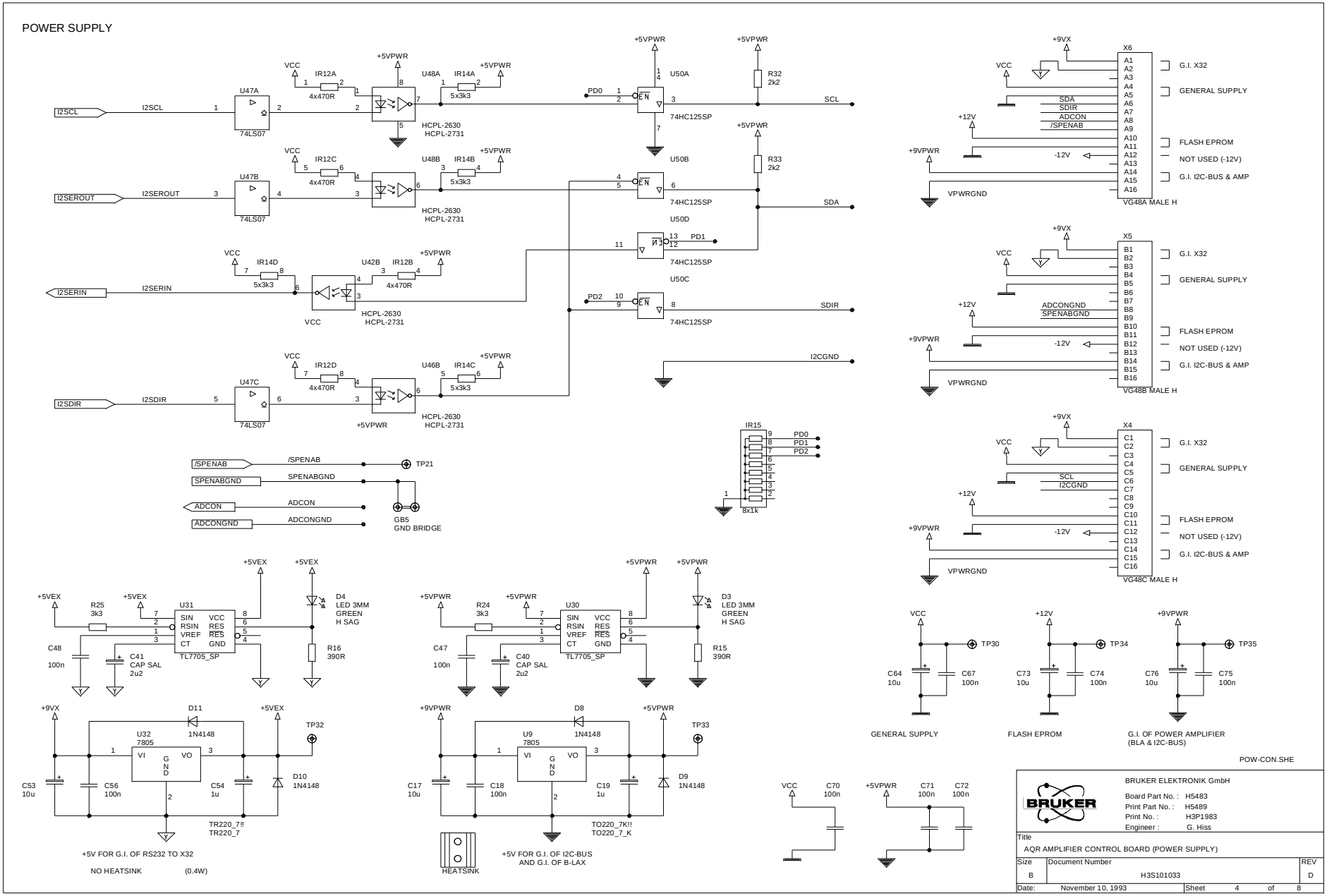
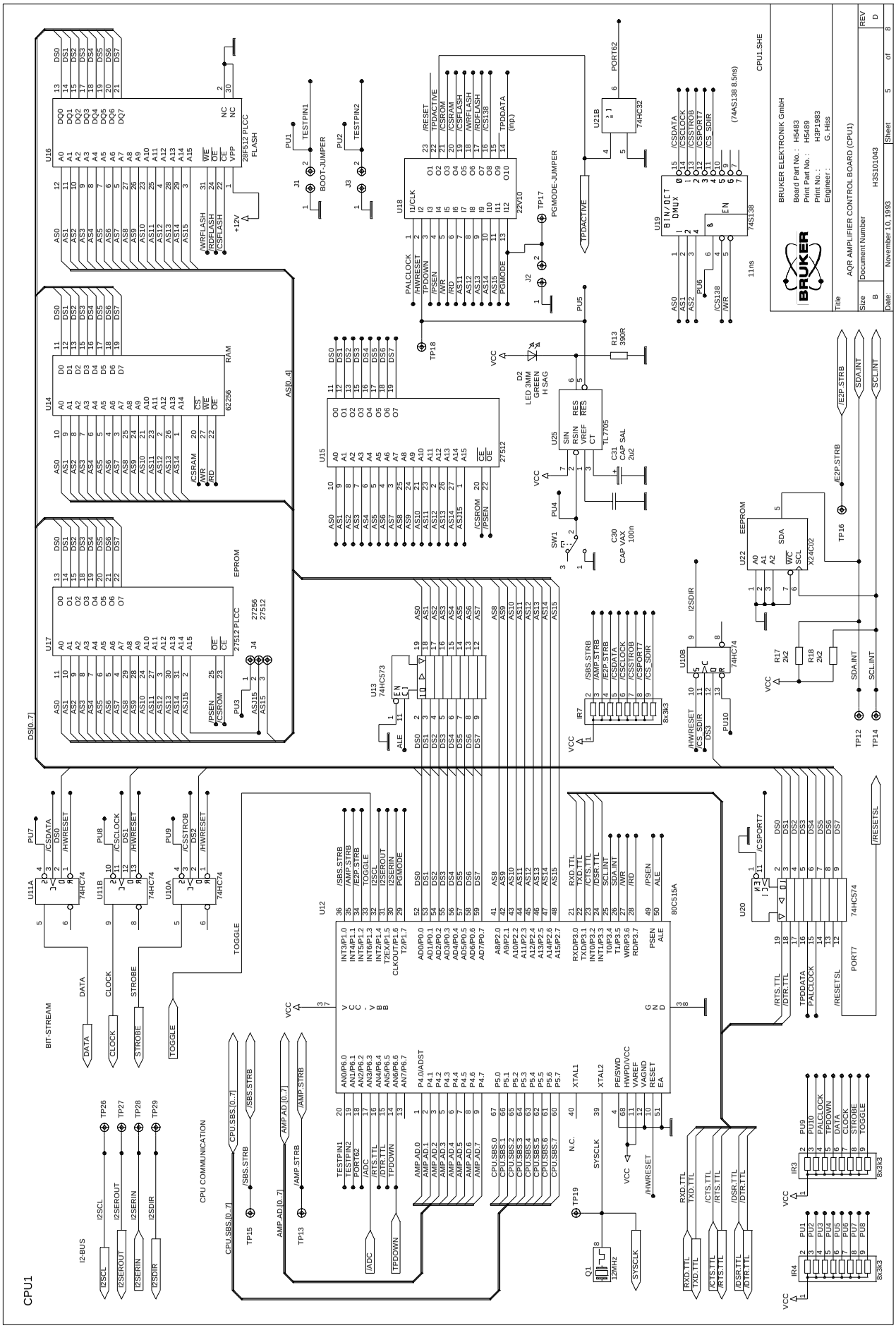


Figure B.4. ACB - power supply

Figure B.5. ACB - CPU1



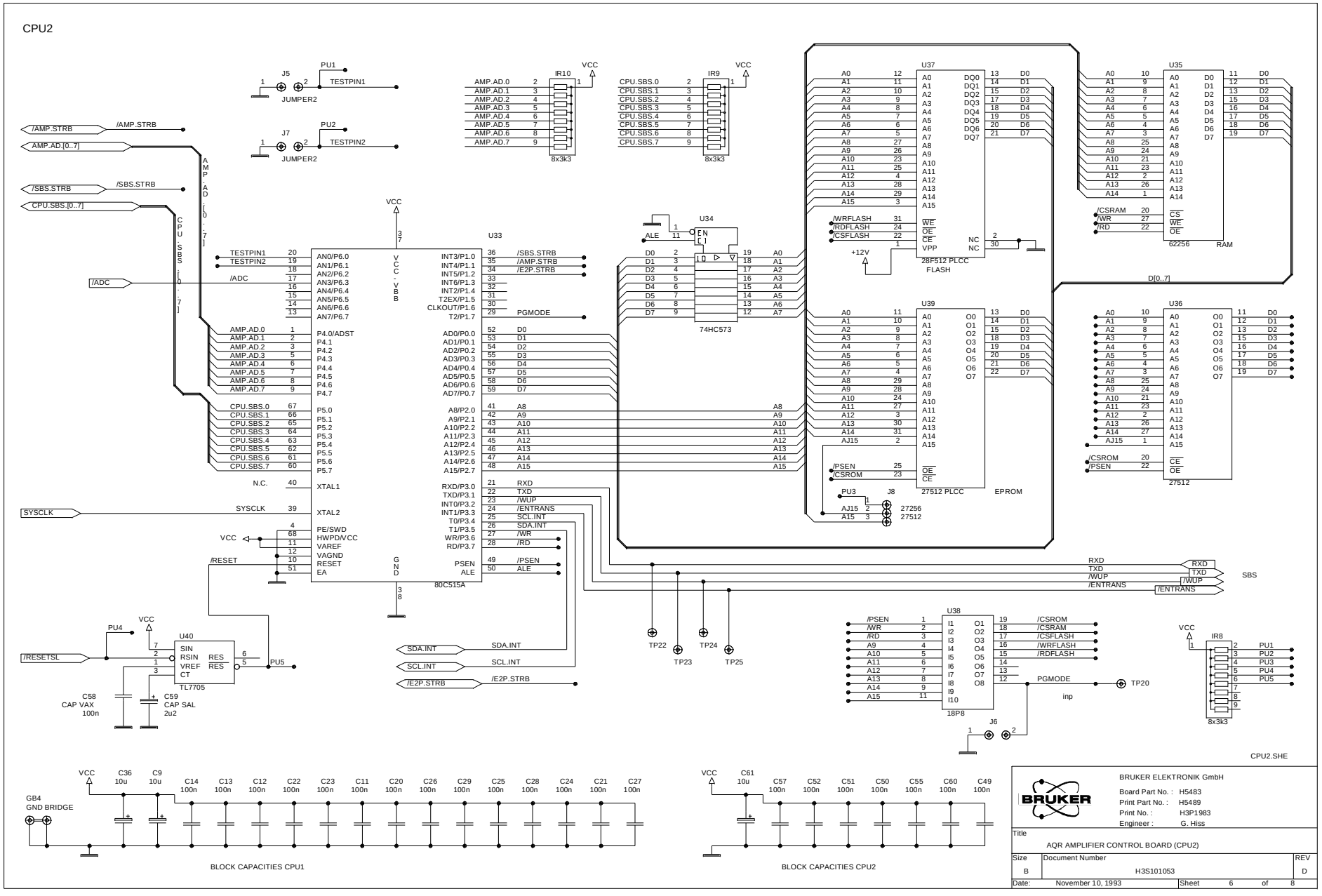


Figure B.6. ACB - CPU2

Figure B.7. ACB - SBS Interface to BLA-Controller

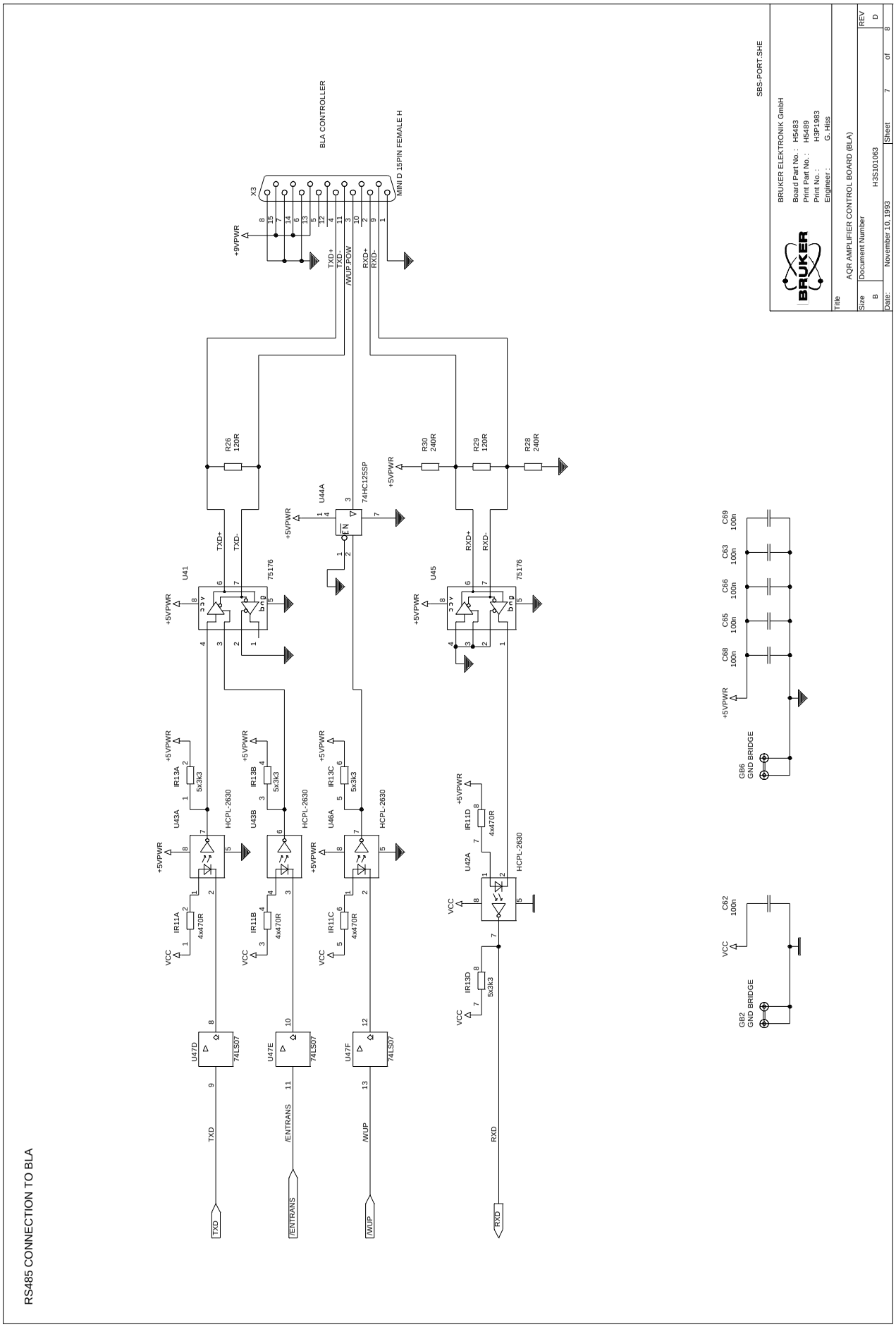
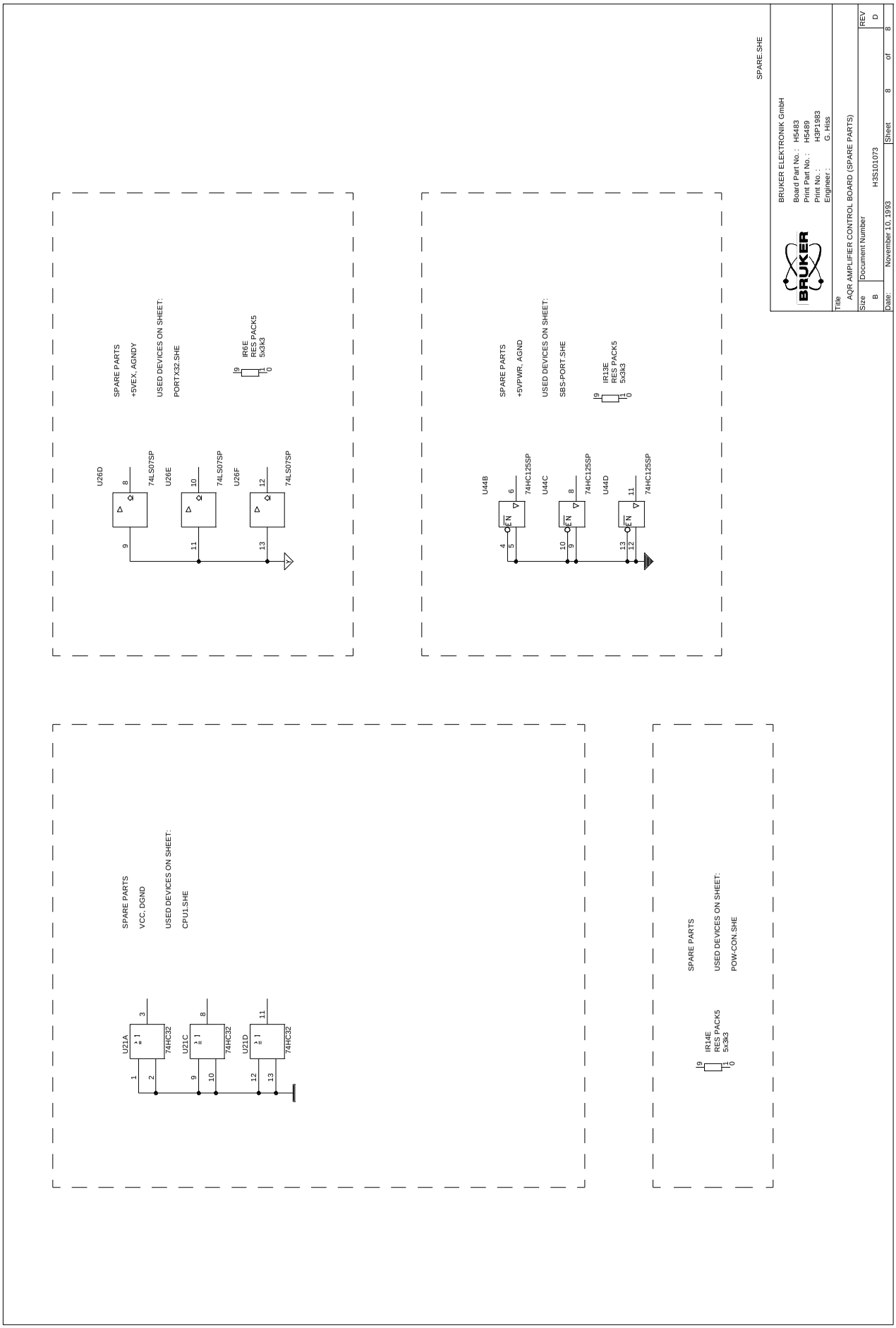


Figure B.8. ACB - spare parts



Figures

Figures

Tables

Tables